

Atria Institute of Technology Bengaluru – 560024

Approved by AICTE | Affiliated to VTU Belagavi | Accredited by NAAC

Department of Computer Science and Engineering

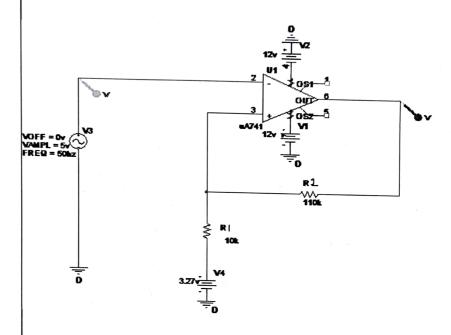
Date: 30-07-2019

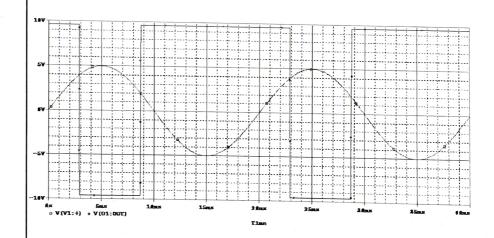
DETAILS OF THE INNOVATIVE TEACHING METHODS USED BY THE FACULTY

Academic Year	2019-20, ODD SEM			
Subject Name and Subject Code	Analog & Digital Electronics, 18CS33			
Faculty Name	Hemalatha K N/Sumitha B			
Semester	III			
Name of the Innovative Teaching Methods used	Hands-On Session On "PSPICE Software To Simulate A Circuit"			
Short Description of the Innovative Teaching Activity.	In order to ensure a successful circuit design and mitigate costly and potentially dangerous design flaws, careful planning and evaluation must occur at every stage of the circuit design process. Circuit simulation provides a cost-effective and efficient method for identifying faults before moving to the more expensive and time-consuming prototyping stage. Including simulation in the design process reduces design errors and speeds the design cycle by allowing you to predict and better understand circuit behavior. The main purpose of simulation is to predict and understand the behavior of electronic circuits. PSpice is a program that simulates electronic circuits on your PC. Intended Students: 2 nd year students Limitations of simulation: While a prototype helps you to verify and validate your design in the real world, simulation helps you catch design errors before spending money and time on prototyping.			

	Orcad 9.2 Lite Edition Installation:				
	 Insert Cadence CD into CD-ROM drive Select Products to install Capture – Schematic entry application – it must be installed Capture CIS – Should be grayed out. PSpice – For conducting mixed-signal analog and digital simulations Layout– For creating PC Board layouts from schematics 				
	Then follow the instructions as it appears on the monitor and complete the installation The steps to simulation:				
	 Create a simulation project Draw schematic to simulate Establish a simulation profile Set up simulation type Simulate circuit Analyze results in Probe 				
Number of students got benefited.	40				
Number of students involved in the activity.	54				
Venue of the Activity	ADE Lab				
Date of the Event	29/07/2019@10 AM				
Whether the work can be Reproduced and Reviewed.	YES				
Details are available in the college website.	YES				

Photograph for the event









Contents of the Event	Students simulated the circuits using Pspice software and explored practical working of theoretical circuits							ored the	
									1:66 mant
Impact Analysis after using	Student's intere	est has l	been in	creased	in desi	gning tr	ie circu	it in a	anterent
this Innovative Teaching	practical way								
Methods used.									
Feedback from the students	Timestam 1. Knowle	2 Diagon	2 14/hich t	E Evnecta	A Whethe	5 How do	6. How do	7.Is the	Fa 8.Pace of
	2019/07/2 Some Hov	3.Please C	Cates	Good	Kinda	More fun	. More bre	Fairly	Satisfacto
	2019/07/2 Some Hov 2019/07/2 Definelty	Very Good	Cathode F						Good
	2019/07/2 Definelty		Realizing		Yes becau	By having	No proble	Yes	Very Goo
	2019/07/2 Some Hov		Basics gat		Yes			Yes	Good
	2019/07/2 Some Hov		Logical ga		Yes	Its good n	Nothing	Yes	Satisfacto
	2019/07/2 Definelty		ADE		it should l	They shou	They shou	Yes	Satisfacto
	2019/07/2 Definelty		Lab	Good	Yes	-	-	Yes	Satisfacto
	2019/07/2 Definelty		Gates	Satsfactor	Can be	With mor	More inte	Fairly	Satisfacto
	2019/07/2 Definelty	Very Good	Analog an	Good	Yes	Yes	Better inv	Yes	Good
	2019/07/2 Definelty	Very Good	How to pr	Very Good	Yes	By presen		Yes	Good
	2019/07/2 Definelty	Average	Introducti	Satsfactor	Ya of cour	Some acti	More exp	Fairly	Satisfacto
	2019/07/2 Definelty	Average	the introd	Satsfactor	yes but w	by making	by motiva	Fairly	Satisfacto
	2019/07/2 Definelty		ADE Lab	Very Good	Yes,becau	By conduc	By more c	Yes	Good Satisfacto
	2019/07/2 Definelty			Satsfactor					Good
	2019/07/2 Definelty		Logic gate				Better cor	_	Good
	2019/07/2 Definelty			Very Good	YES Yes should	Yup Rotter eg	By giving	Yes	Good
	2019/07/2 Definelty		Gates Lab				More inte		Good
	2019/07/2 Definelty		Logic Gate				With mon		Satisfacto
	2019/07/2 Definelty 2019/07/2 Definelty						I don't kno		Very Goo
	2019/07/2 Definelty		Ic				With some		Satisfacto
	2019/07/2 Definelty		Analog		Yes	No	No	Yes	Good
	2019/07/2 Definelty		Connectio	Good	Yes	By keepin	It was goo	Yes	Good
	2019/07/2 Definelty	Good	Digital ele	Very Good	Yesbeca	By giving I	By involvi	Yes	Good
	2019/07/2 Definelty	Good	Digital ele				By involvi		Good
	2019/07/2 Definelty								Good
	2019/07/2 Definelty						Better equ		Good
	2019/07/2 Definelty					, manager as array of the course of the course	By involvi	Name of the last o	Very Goo
	2019/07/2 Definelty		Almost all		Yes , beca			Yes Yes	Good Vegy Goo
	2019/07/2 Definelty			Very Good	res,pecau c		No idea No idea		Very Goo Good
	2019/07/2 Definelty		Digital ele E-Homo	φη.			and the second		
Relevance to PO and PSO	PO3,PO5,PO9							11	
Any comments or Suggestions	The content sh	nould b	e readil	y made	in colle	ge web	site		
			•	-		_			
from the Programme Co- ordinator									

Signature of the Faculty	Signature of the HOD
(Hennalallia K.N.)	COMPUTER SELENCE ENGS COMPUTER SELENCE ENGS ATRIA INSTITUTE OF TECHNOLOGY ATRIA INSTITUTE